AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) A processing device comprising:

one or more resources within a node;

a plurality of peripheral bus interfaces coupled to the one or more resources and coupled to a peripheral bus fabric to support resource sharing with a plurality of other processing devices of other nodes when the other processing devices are coupled to the peripheral bus fabric;

a node identification (ID) register including primary routing resources programmable with a plurality of addresses to determine a primary routing ~~of a~~ for a plurality of peripheral bus transactions among the plurality of peripheral bus interfaces based upon a destination address ~~of the~~ for each respective peripheral bus transaction, the plurality of peripheral bus transactions being types of transactions including packet data transfer transactions, input/output transactions with input/output devices and cache coherency transactions to maintain cache coherency with other nodes; and

the node ID register also including a node routing table containing one or more override indications to determine ~~one or more~~ an alternate override routing ~~of the~~ for a particular peripheral bus transaction over the primary routing ~~and~~, in which the primary routing for the particular peripheral bus transaction is overridden by ~~one or more~~ the alternate override routing when the destination address and a type of transaction for the particular peripheral bus transaction is ~~indicated~~ identified by one or more override indications in the node routing table for alternate routing.

2. (currently amended) The processing device of claim 1 wherein the processing device determines a node ID of a destination device based upon a set of most significant bits of

the destination address of ~~the~~ each respective peripheral bus transaction.

3. (previously presented) The processing device of claim 1 wherein the processing device is to ignore the alternate override routing based upon programmed contents of the node ID register.

4. (currently amended) The processing device of claim 1 wherein ~~one alternate override routing indication applies to the peripheral bus transaction~~ when the particular peripheral bus transaction is a cache coherency peripheral bus transaction, the override routing indication is used to route the particular peripheral bus transaction through an alternate route instead of a primary route.

5. (currently amended) The processing device of claim 1 wherein ~~one alternate override routing indication applies to the peripheral bus transaction~~ when the particular peripheral bus transaction is an input/output peripheral bus transaction, the override routing indication is used to route the particular peripheral bus transaction through an alternate route instead of a primary route.

6. (currently amended) The processing device of claim 1 wherein ~~a first alternate override routing indication applies to the peripheral bus transaction~~ when the particular peripheral bus transaction is a cache coherency peripheral bus ~~transactions~~ transaction, a first override routing indication is used to route the particular peripheral bus transaction through a first alternate route instead of a primary route, and ~~a second alternate override routing indication applies to the peripheral bus transaction~~ when the particular peripheral bus transaction is an input/output peripheral bus transaction, a second override routing indication is used to route the particular peripheral bus transaction through a second alternate route instead of the primary route.

7. (currently amended) The processing device of claim 6, wherein the alternate override routing is selectively disabled with regard to the cache coherency peripheral bus ~~transactions and/or~~ transaction or the input/output peripheral bus ~~transactions~~ transaction.

8. (canceled)

9. (previously presented) The processing device of claim 1, wherein each of the override indications also indicates either a primary port or a secondary port of one of the peripheral bus interfaces selected for override routing of the peripheral bus transaction.

10. (previously presented) The processing device of claim 1 wherein the node routing table includes an entry for each of a plurality of processing devices, each entry comprising:

an override bit corresponding to input/output peripheral bus transactions;

a primary/secondary port indication corresponding to input/output peripheral bus transactions;

an override bit corresponding to cache coherency peripheral bus transactions; and

a primary/secondary port indication corresponding to cache coherency peripheral bus transactions.

11-28. (canceled)

29. (currently amended) A method for operating a processing device having one or more resources and a plurality of peripheral bus interfaces that are operable to couple the one or more resources of a node to one or more other processing devices of other nodes via a peripheral bus fabric, the method comprising:

receiving a peripheral bus transaction at the processing device, the peripheral bus transaction being a type of transaction including a packet data transfer transaction, input/output transaction with input/output devices or cache coherency transaction for maintaining cache coherency with other nodes;

determining a primary routing of the peripheral bus transaction among the plurality of peripheral bus interfaces based upon a destination address of the peripheral bus transaction programmed in a node identification (ID) register;

determining an alternate override routing of the peripheral bus transaction among the plurality of peripheral bus interfaces based upon entries in a node routing table, in which the primary routing for the peripheral bus transaction is used to route the peripheral bus transaction unless overridden by an alternate override routing when the destination address and a type of transaction for the peripheral bus transaction is ~~indicated~~ identified by an override indication in the node routing table; and

routing the peripheral bus transaction among the plurality of peripheral bus interfaces according to the primary routing through a primary route, unless the node routing table indicates an entry to override the primary routing based on the type of transaction for the peripheral bus transaction, in which an alternate route is used to route the peripheral bus transaction.

30. (previously presented) The method of claim 29 further comprising determining a node ID of a destination device based upon a set of most significant bits of the destination address of the peripheral bus transaction.

31. (canceled)

32. (currently amended) The method of claim 29 further comprising applying the alternate override routing to the peripheral bus transaction when the peripheral bus transaction is a cache coherency peripheral bus transaction and to route the peripheral bus transaction by the alternate route.

33. (currently amended) The method of claim 29 further comprising applying the alternate override routing to the peripheral bus transaction when the peripheral bus transaction is an input/output peripheral bus transaction and to route the peripheral bus transaction by the alternate route.

34. (currently amended) The method of claim 29 further comprising applying ~~the~~ a first alternate override routing to the peripheral bus transaction when the peripheral bus transaction is ~~either~~ a cache coherency peripheral bus transaction to route the peripheral bus transaction by a first alternate route ~~or~~ and applying a second alternate override

routing to the peripheral bus transaction when the peripheral bus transaction is an input/output peripheral bus transaction to route the peripheral bus transaction by a second alternate route.

35. (currently amended) The method of claim 34, further comprising applying the primary routing to a packet data peripheral bus transaction and to route the packet data peripheral bus transaction by the primary route.